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LETTER

A High-Efficient Transformer Using Bond Wires for Si RF IC

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SUMMARY This paper presents a design of a monolithic transformer using bond wires. The proposed transformer structure has several advantages such as high power handling and high efficiency. It shows that the measured insertion loss at the 1.9 GHz range is −1.54 dB (70%), which is higher than the spiral transformer of the same size. Also, it shows a phase error of less than 1 degree.

key words: *CMOS RF integrated circuit, monolithic transformers, bond wires, balun*

1. Introduction

A CMOS is the most popular device for a monolithic microwave integrated circuit. Transformers are an essential component in RFIC; thus, there have been prior attempts to integrate transformers [1]. However, several factors limit the performance of on-chip transformers. First, the conductor loss associated with the metal windings is often significant. Second, the substrate is a major source of loss due to the conductive nature of Si. Furthermore, high DC currents need an extra design consideration on account of electromigration effect.

In this paper, we propose a new on-chip transformer structure utilizing the characteristics of bond wires. They have high quality factor (Q factor) and can bear higher DC currents inherently. These allow for useful performance characteristics.

2. Transformer Design

Integrated passive devices must reside near a conductive Si substrate. One of the major losses is generated by eddy currents due to the time-varying magnetic fields penetrating the substrate. Generally, eddy currents loss is inevitable in a spiral windings case since the magnetic fields are vertical to the substrate. As shown in Fig. 1, we propose a 3-dimensional transformer using bond wires that looks like a solenoid.

This feature has three advantages. Firstly, a gold bond wire has a thick diameter, so it shows a higher Q factor than typical metal layers. Secondly, the new transformer structure makes eddy currents loss decrease because the magnetic fields are geometrically parallel to the substrate. Finally, the proposed feature can be integrated with "high- power" passive on Si, such as the combining network at the output of a power amplifier. A bond wire, because of a large diameter (using 1-mil), is almost free from electromigration and metal stress problems.

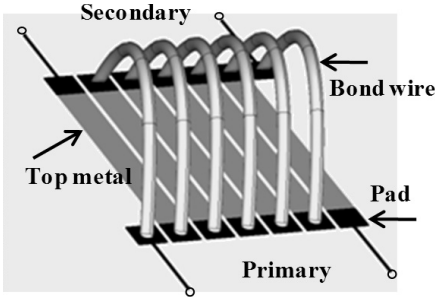

Fig. 1 Perspective view of a proposed transformer using bond wires.

The key design parameters to optimize the efficient performance are the spacing between adjacent bond wires and its loop height. The spacing directly affects the coupling coefficient, which is the key factor to determine the transformer efficiency [2]. The size of pads must be minimized to reduce the distance between wires, which can enhance the coupling coefficient. Another important design factor is to guarantee a high enough loop height for sufficient inductive coupling. The transformer has a maximum efficiency when inductor reactance is an optimum value [2].

3. Simulation and Measurement Results

The transformer is implemented in a standard 0.13-μm 1-poly 8-metal CMOS process with a copper top-metal thickness of 2 μm. The bond wire of 1 mil diameter is used. The optimized transformer size for the best performance at 1.9 GHz is 580 μm × 540 μm including pads. The minimum size of pads is selected by a process design rule. The loop height is 300 μm, optimized for sufficient inductive coupling. Figure 2 shows the microphotograph of the top view and side view. Also, for comparison, the conventional spiral transformer is fabricated in the same process and same area. It consists of three turns of 20-μm-wide top metal with a 3-μm conductor spacing. It shows optimum performance for high power applications. The circuit simulation is verified by using Agilent ADS, and all passive structures and interconnections are simulated using both CST MWS and Agilent Momentum.

Figure 3 shows the simulated Q factor and inductance of the proposed transformer versus the loop height at the

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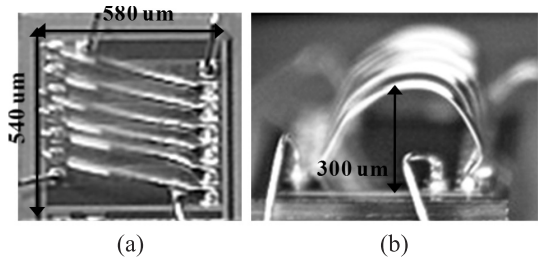

Fig. 2 Chip photograph of the transformer. (a) Top view. (b) Side view.

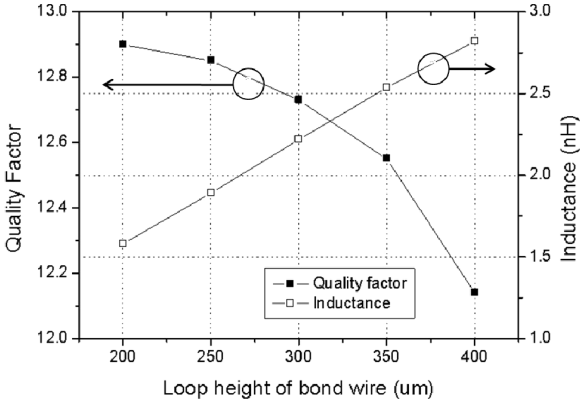

Fig. 3 Simulated Q factor and inductance versus the loop height.

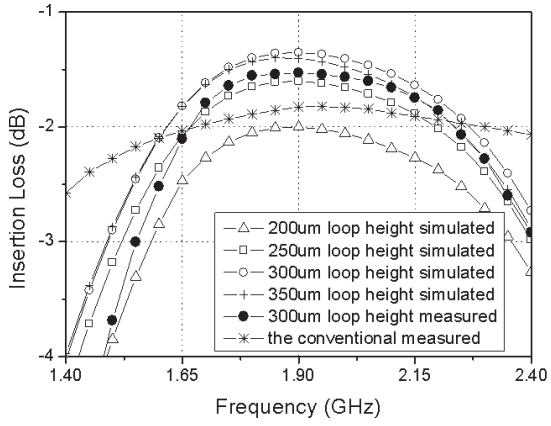

Fig. 4 Simulation and measurement of insertion loss of the proposed and the conventional transformers.

1.9 GHz. It shows that the proposed transformer has Q factor more than 12, while Q factor of the conventional transformer is about 8. It means the path of bond wires has lower resistance than that of metal layers. Figure 4 shows the insertion losses of the proposed and the conventional transformers. In the 300 μm height case, the simulated and

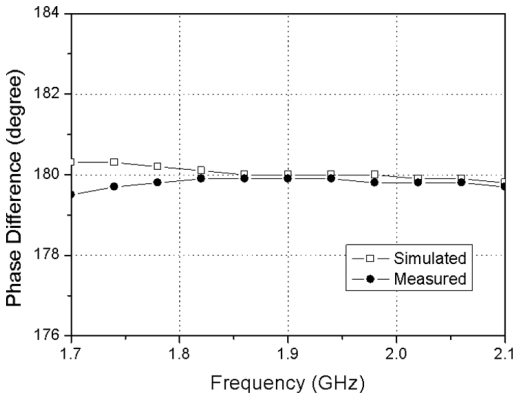

Fig. 5 Frequency response of differential phase output at the secondary.

measured insertion losses at the 1.9 GHz range are −1.35 dB (73%) and −1.54 dB (70%), respectively. On the other hand, the simulated and measured insertion losses of the spiral transformer are −1.55 dB (70%) and −1.8 dB (66%). These results include connector and PCB losses, which is for resonance tuning. Figure 5 shows the simulated and measured phase difference versus the frequency. The differential-port signals are ideally 180 degrees phase difference. It shows that the phase error at the secondary is less than 1 degree.

4. Conclusion

The proposed transformer was fabricated using 0.13-μm CMOS technology. We have introduced the design, simulation and measurements. The proposed structure has the advantages of high efficiency and less metal stress problems. The measured insertion loss at the 1.9 GHz range is −1.54 dB (70%), including PCB loss. This can be easily integrated with PAs and also used for balun.

Acknowledgments

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